ADQ32 Datasheet

The ADQ32 is a high-end 12-bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ32 features:

- **One and Two analog input channels**
- **5 and 2.5 GSPS per channel**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**

1 ADQ32 INTRODUCTION

1.1 Features

- One and two analog input channels
- 5 and 2.5 GSPS sampling rate per channel
- 12 bits vertical resolution
- DC-coupled with 1 GHz bandwidth
- Programmable DC-offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 GBytes data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- 7 GByte/s peer-to-peer data streaming to GPU
- Data interface PCIe Gen3 x8

1.2 Applications

- Swept-Source Optical Coherence Tomography (SS-OCT)
- Time-of-flight Mass Spectrometry
- Distributed Optical Fiber Sensing
- LIDAR

1.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

1.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ32 offers a variety of options for efficient system design:

Streaming to GPU
ADQ32 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ32 supports up to 7 GByte/s to host PC. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ32 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

2 TECHNICAL DATA

Technical parameters are valid for ADQ32 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A and B)

Parameter	Condition	Unit	Min	Typical	Max
Basic parameters					
Number of channels	2 channels mode			2	
Sampling rate per channel	2 channels mode	Gsample/s		2.5	
Number of channels	1 channel mode			1	
Sampling rate	1 channel mode	Gsample/s		5	
Bandwidth	-3dB	GHz		1	
Input range		Vpp		0.5	
Input impedance		Ω		50	
Coupling				DC	
Connector type				SMA	
Programmable DC-offset					
DC-offset range		V	-0.25		+0.25
AC performance 2 channels mode					
Cross talk	< 1 GHz	dBFS		-70	
Noise power density	0 to 1.25 GHz	dBFS/√Hz		-148	
SNR	260 MHz, -1dBFS	dBc		55	
SFDR	260 MHz, -1dBFS	dBc		66	
ENOB relative full scale	10 MHz, -1dBFS	bits		9	
ENOB relative full scale	260 MHz, -1dBFS	bits		8.9	
ENOB relative full scale	810 MHz, -1dBFS	bits		8.5	
AC performance, 1 channels mode, no FIR filter					
SNR	260 MHz, -1dBFS	dBc		54	
SFDR	260 MHz, -1dBFS	dBc		65	
ENOB relative full scale	10 MHz, -1dBFS	bits		8.9	
ENOB relative full scale	260 MHz, -1dBFS	bits		8.8	
ENOB relative full scale	810 MHz, -1dBFS	bits		8.5	
AC performance, 1 channels mode, FIR filter[1]					
SNR	260 MHz, -1dBFS	dBc		57	
ENOB relative full scale	10 MHz, -1dBFS	bits		9.2	
ENOB relative full scale	260 MHz, -1dBFS	bits		9.2	
ENOB relative full scale	810 MHz, -1dBFS	bits		9.1	

[1] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

Table 2 Clock generator and front panel CLK connector.

Parameter	Condition	Unit	Min	Typical	Max
Internal clock reference					
Frequency		MHz		10	
Accuracy		ppm		±3 ±1/year	
Internal sampling clock generator[2]					
Frequency range 1	2 channels	MHz	2440	2500	2500
Frequency range 2	2 channels	MHz	1840		1970
Frequency range 1	1 channel	MHz	4880	5000	5000
Frequency range 2	1 channel	MHz	3680		3940
External clock reference input (from front panel CLK connector)[3]					
Frequency		MHz	1	10	500
Frequency [4]	Jitter cleaner enabled	MHz	10 -10 ppm	10	500 +10 ppm
Frequency	Delay line used	MHz		10	100
Delay line tuning range		ps		500	
Signal level		Vpp	0.5		3.3
Input impedance	AC	Ω		50	
Input impedance	DC	Ω		10k	
Input impedance (high) [5]	AC	Ω		200	
Clock reference output (on front panel CLK connector)[6]					
Frequency		MHz		10	
Signal level	Into 50-Ω load	Vpp		1.2	
Output impedance	AC	Ω		50	
Output impedance	DC	Ω		10k	
External direct sampling clock input (from front panel CLK connector)[7]					
Frequency [8]		MHz	1000	2500	2500
Signal level		Vpp	0.5		3.3
Impedance	AC	Ω		50	
Impedance	DC	Ω		10k	
Physical connector label CLK					
Connector type				SMA	

[2] The internal clock generator can generate frequencies in 2 different ranges.
[3] Using a clock reference from an external source to synchronize the ADQ32 to the external source.
[4] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[5] Software-selectable high-impedance mode.
[6] The internal clock reference of the ADQ32 is made available to synchronize external equipment.
[7] Using an external clock while bypassing the internal clock generator.
[8] In one channel mode, the sampling frequency is 2 time the external clock frequency.

Table 3 Front panel TRIG connector

Parameter	Condition	Unit	Min	Typical	Max
Connector				SMA	
Used as input (trigger in or GPIO)					
Impedance	DC	Ω		50	
Impedance (high) [9]	DC	Ω		500	
Signal level	50-Ω mode	V	-0.5		3.3
Adjustable threshold	50-Ω mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution [10]	As trigger	ps		50	
Update rate [10]	As GPIO	MHz			156.25
Used as output (trigger out or GPIO)					
Impedance	DC	Ω		50	
Output level high VOH	Into 50-Ω load	V	1.8		
Output level low VOL	Into 50-Ω load	V			0.1
Pulse repetition frequency		MHz			156.25

Table 4 Front panel SYNC connector (sync is a trigger signal with limited timing resolution)

Parameter	Condition	Unit	Min	Typical	Max
Connector				SMA	
Used as input (sync in or GPIO)					
Impedance	DC	Ω		50	
Impedance (high) [9]	DC	Ω		500	
Signal range	50-Ω mode	V	-0.5		3.3
Adjustable threshold	50-Ω mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution [10]	As trigger	ns		3.2	
Update rate [10]	As GPIO	MHz			156.25
Used as output (sync out or GPIO)					
Impedance	DC	Ω		50	
Output level high VOH	Into 50-Ω load	V	1.8		
Output level low VOL	Into 50-Ω load	V			0.1
Pulse repetition frequency		MHz			156.25

[9] Software-selectable high-impedance mode.
[10] Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 5 Front panel GPIO connector

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
Used as input					
Impedance		Ω		50	
Impedance (high) [9]		kΩ		10	
Input level high VIH		V	2		
Input level low VIL		V			0.8
Update rate [10]		MHz			156.25
Used as output					
Output Impedance		Ω		50	
Output level high VOH	Into 50-Ω load	V	1.5		
Output level high VOH	No load	V	3.2		
Output level low VOL	Into 50-Ω load	V			0.1
Output level low VOL	No load	V			0.1
Update rate [10]		MHz			156.25

Table 6 Environment and mechanical parameters

Parameter	Condition	Unit	Min	Typical	Max
Power and temperature					
Power consumption [11] [12]	FWDAQ	W		30	
Power supply		V	10.8	12	13.2
Operating temperature	At fan inlet	°C	0		45
Size					
Width				1 slot	
Length		mm		225.7	
Height		mm		111.2	
Compliances					
RoHS3				Yes	
CE				Yes	
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c)				

[11] Power consumption depends on firmware option and use case.

[12] Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

Table 7 Data acquisition

Parameter	Condition	Unit	Min	Typical	Max
Re-arm time		ns			20
Acquisition memory (Data FIFO)	Shared by all channels	GBytes		8	
Record length		samples	16		2^{31}
Pre-trigger[13]		samples	0		16 360
Length granularity, pre-trigger		samples	8		
Trigger delay[14]		samples	0		2^{32}-8
Length granularity, trigger delay		samples	8		

Table 8 Data transfer

Parameter	Unit	Value
Supported versions of data transfer standard PCIe		Gen1 Gen2 Gen3
Supported number of lanes		1 4 8
Data rate to CPU sustained with headers	GByte/s	5
Data rate to CPU sustained without headers	GByte/s	7
Data rate to GPU sustained without headers	GByte/s	7
Data rate peer-to-peer to GPU sustained without headers	GByte/s	7

Table 9 Software support

Parameter	Value
Operating system	Windows 10 Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[13] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[14] Trigger delay is set by assigning the parameter “horizontal offset” a positive value

3 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ32 features an advanced machine for flow control, synchronization and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

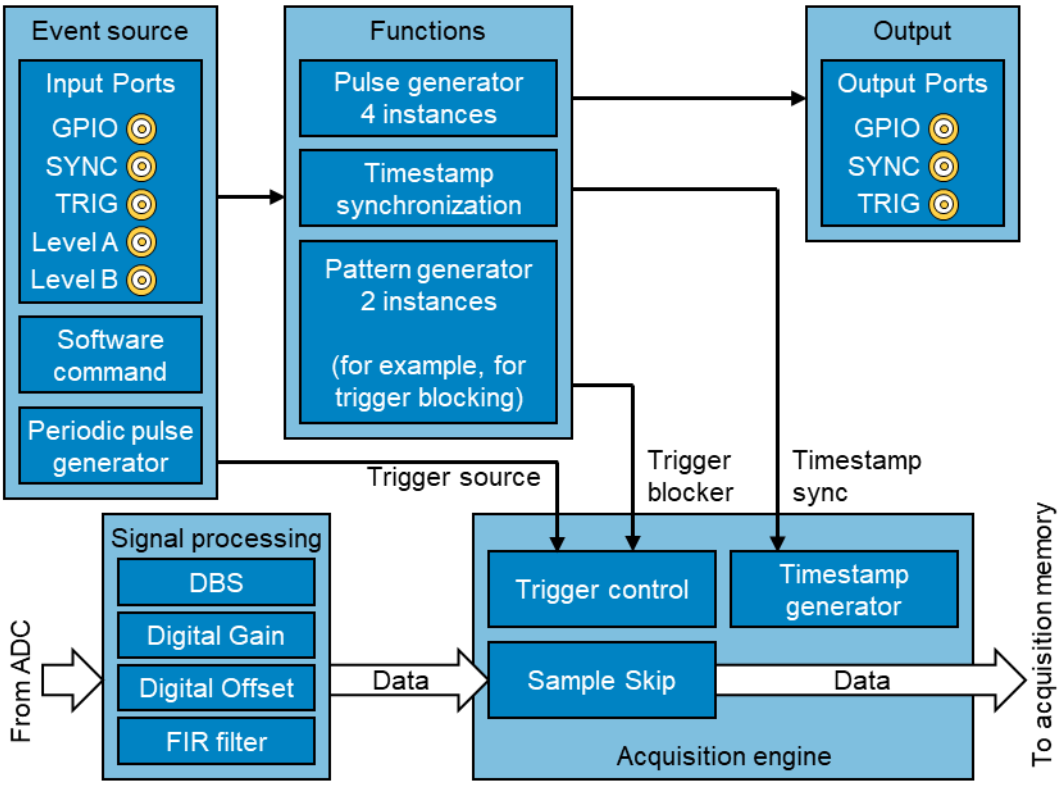


Figure 1 Flow control and synchronization block diagram.

Table 10 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 11 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
Event sources Signals for real-time control of activities in the firmware of ADQ32.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
Functions Included operations for real-time control of activities in the firmware of ADQ32.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 12 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp sync Control the time of the ADQ32.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 13 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Streaming with header Streaming without header	

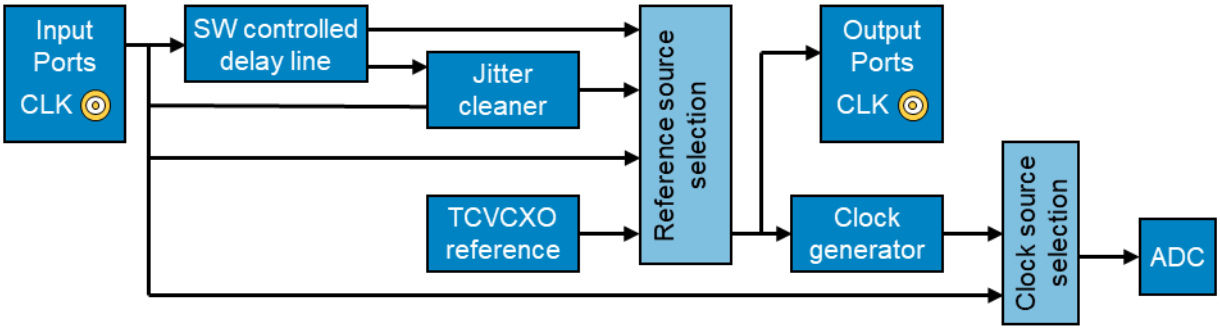


Figure 2 Clock generation block diagram.

Table 14 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

4 CHANGING NUMBER OF CHANNEL

Changing from 2 channels to 1 channel is done by changing firmware image in the FPGA. Both firmware images are available on the ADQ32 digitizer. Use the software tool ADQAssist to change boot image. Changing firmware requires power cycle PC for the PCIe to enumerate.

5 ABSLOUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Parameter	Condition	Unit	Min	Max
Power supply to GND		V	-0.4	14
Operating temperature		°C	0	45
Analog in to GND		V	-1.75	+1.75
TRIG to GND	50-Ω mode	V	-2	5
SYNC to GND	50-Ω mode	V	-2	5
TRIG to GND	500-Ω mode	V	-2	6
SYNC to GND	500-Ω mode	V	-2	6
CLK REF to GND AC amplitude		Vpp		5
CLK REF to GND DC-level		V	-5	5
GPIO to GND		V	-1.5	5

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

6 TYPICAL PERFORMANCE

6.1 Frequency response

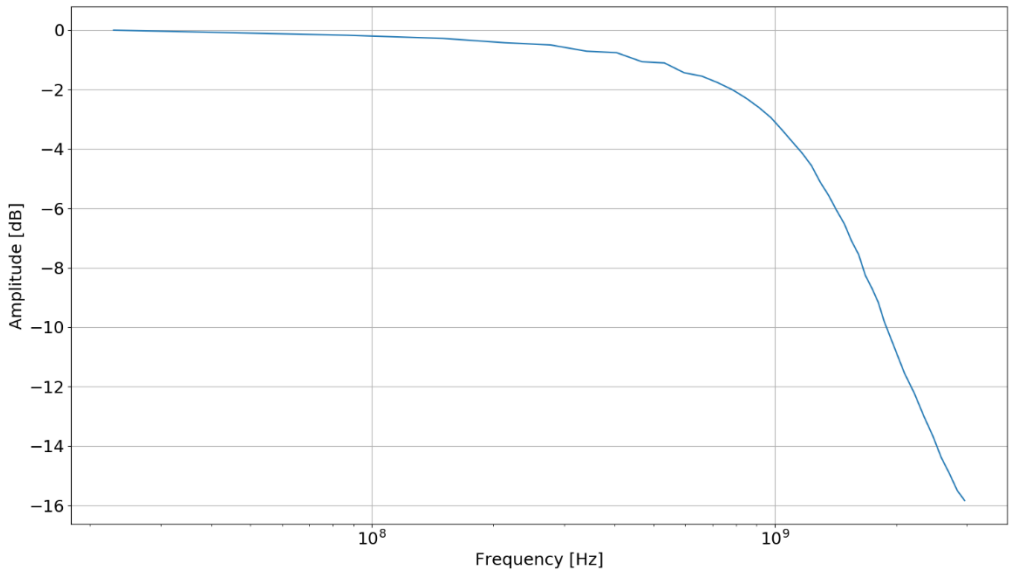


Figure 3 Frequency response, typical performance.

6.2 FFT

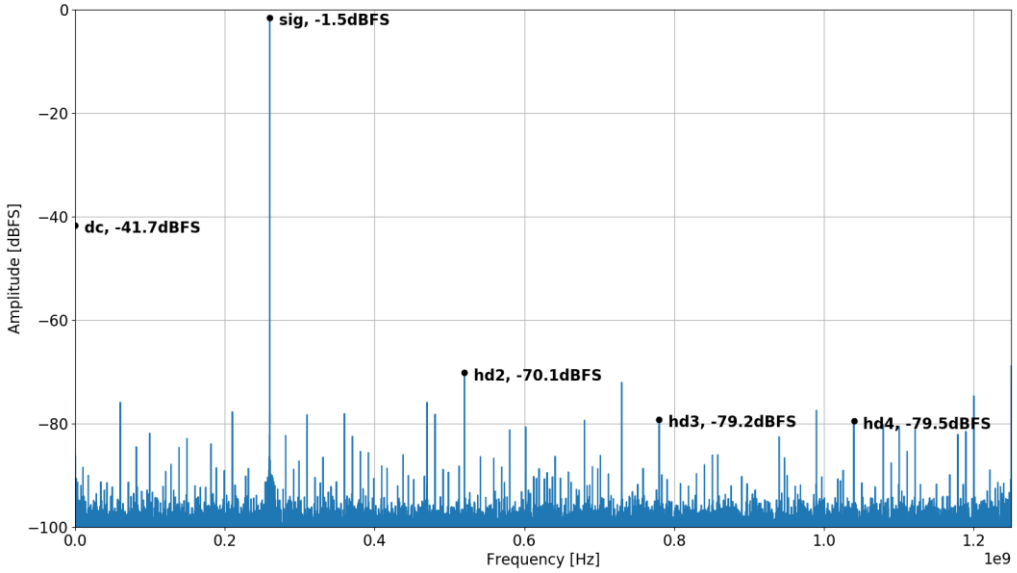


Figure 4 FFT typical performance 2.5 GSPS.

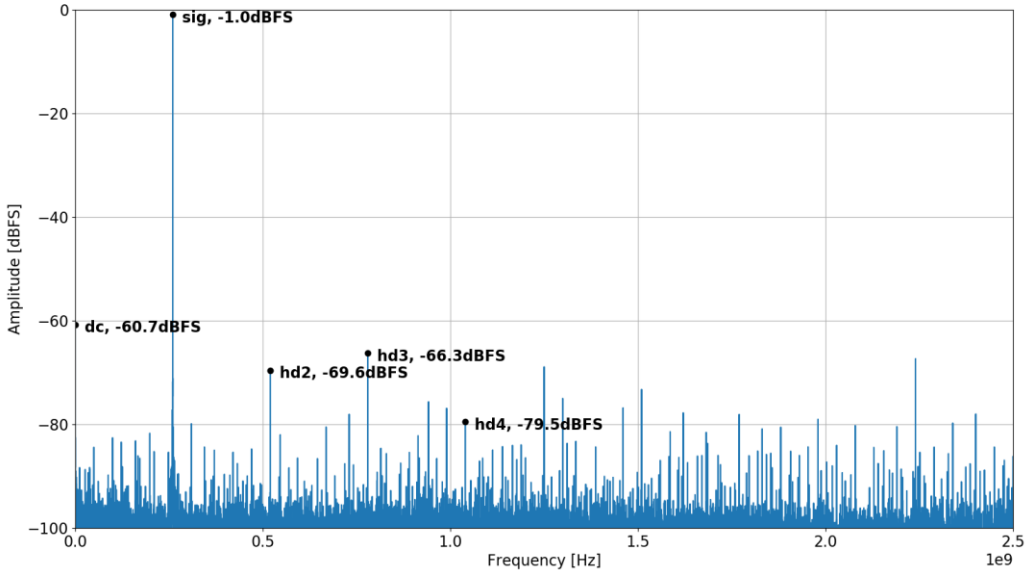


Figure 5 FFT typical performance at 5 GSPS

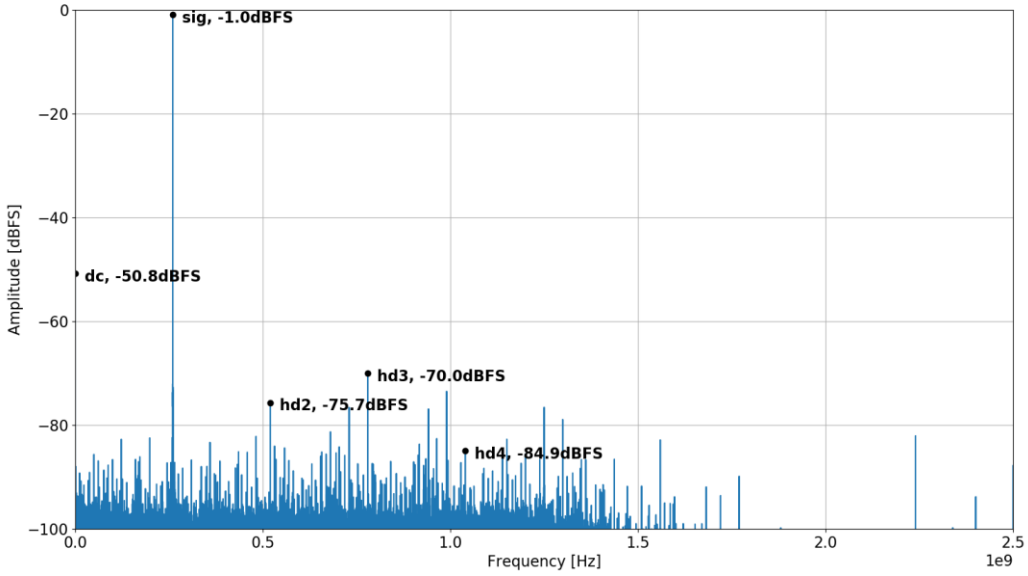


Figure 6 FFT typical performance 5 GSPS, using digital FIR filter.

7 BLOCK DIAGRAM

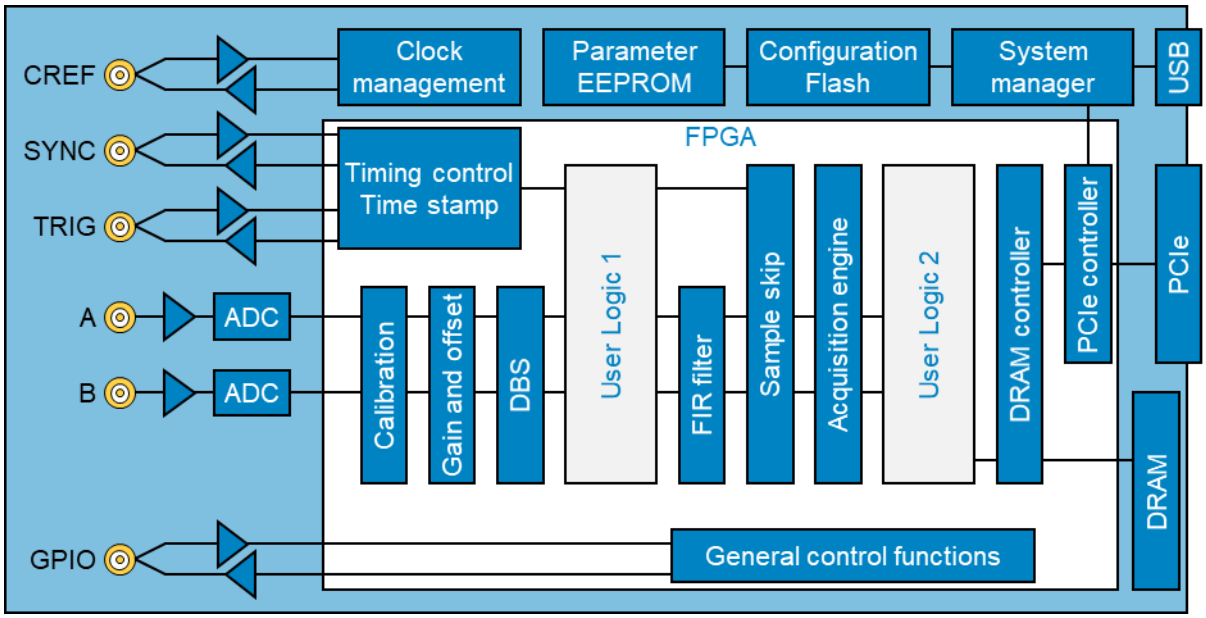


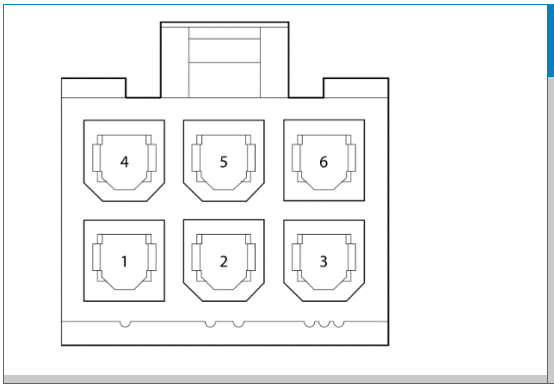
Figure 7 Block diagram.

Figure 7 shows a block diagram of the ADQ32. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

8 HOST PC INTERFACE PCIE

The ADQ32-PCIe is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 8. A suitable connector is for example Molex 45559-0002.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense (Ground)
6	Ground

Figure 8 Power supply connection. Cable connector, looking into the connector end.

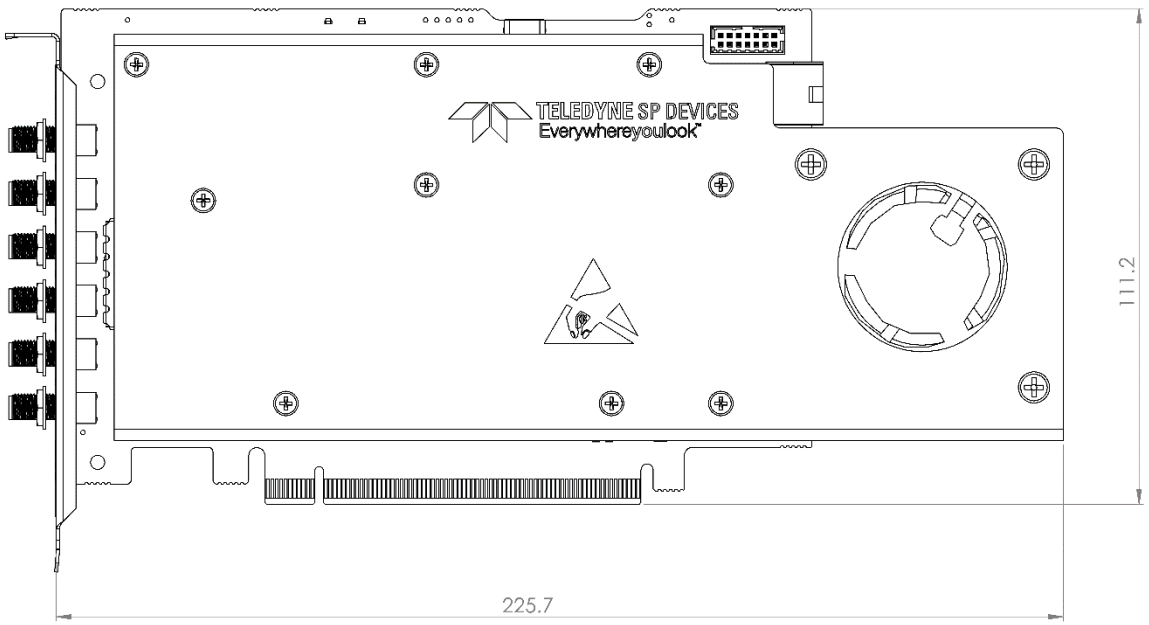


Figure 9 Mechanical drawing

Figure 10 ADQ32 photo

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